

What is claimed is:

1        1. A method for performing power distribution analysis for I/O circuits in an  
2 integrated circuit (IC) design, said I/O circuits having defined placement locations within  
3 a power distribution network of said design, comprising the steps of:

4            a) calculating maximum and average currents for each of said I/O circuits,  
5 and an average logic current demand per node;

6            b) creating a resistance model of said power distribution network comprising  
7 nodes and resistors corresponding to points on buses of said network and resistivities  
8 corresponding to said points;

9            c) indexing each of said I/O circuit currents and said average logic current  
10 demand per node to the node in said model closest to the corresponding I/O circuit  
location;

11            d) solving the resistance and current source model resulting from step (c) for  
12 voltages at the nodes; and

13            e) outputting the results.

1        2. The method of claim 1, further comprising:

2            (f) comparing said results against specified voltage drop (IR) and  
3 electromigration (EM) limits of said design to identify violations of said limits; and

4            (g) changing said I/O circuit placement locations to correct said violations.

1        3. The method of claim 2, further comprising

2 repeating steps (a) - (g) until step (f) does not identify any violations.

1        4. The method of claim 1, wherein said design utilizes an area-array type I/O  
2 circuit distribution.

1        5. The method of claim 1, wherein said design utilizes a peripheral type I/O  
2 circuit distribution.

1           6.     The method of claim 1, wherein step (d) uses a sparse matrix solver.

1           7.     A method comprising:

2                 establishing a distribution of I/O circuits in a power distribution network of an IC  
3     design;

4                 generating a resistance model comprising resistivities at nodes corresponding to  
5     said network;

6                 relating currents of said I/O circuits and an average logic current demand per node  
7     to nodes in said resistance model;

8                 solving for voltages at said nodes in terms of said resistivities, I/O circuit currents  
9     and average logic current demand per node;

10                 identifying ones of said voltages not in compliance with IR and EM limits of said  
11     design; and

12                 re-arranging said distribution to bring said identified voltages into compliance.

1           8.     The method of claim 7, further comprising adjusting a granularity of said  
2     resistance model for a desired accuracy of said model.

1           9.     The method of claim 7, further comprising using lumped resistance values  
2     to represent routing layers of said design in said model.

1           10.    The method of claim 7, wherein said solving step comprises:

2                 formulating a conductance matrix from said resistance model and a current matrix  
3     from said I/O circuit currents and average logic current demand per node;

4                 calculating voltages at said nodes using relationships between said conductance  
5     matrix and said current matrix established by said relating step.

1           11.    The method of claim 7, wherein said identifying step comprises:

2                 comparing said voltages against a design rule specifying an allowable variation of  
3     said voltages as a percentage of a supply voltage.

1           12. The method of claim 7, wherein said step of generating a resistance model  
2 comprises:

3           repeating a bus pattern by a repeat factor, said bus pattern including a bus starting  
4 location, a bus width and a bus end.

1           13. A computer-readable medium storing computer-executable instructions, said  
2 instructions when executed implementing a process comprising:

3           from a power distribution network for an IC design, generating a resistance model  
4 comprising resistivities at nodes corresponding to said network;

5           relating currents of I/O circuits connected to said network, and an average logic  
6 current demand per node, to nodes in said resistance model;

7           solving for voltages at said nodes in terms of said resistivities, I/O circuit currents  
8 and average logic current demand per node; and

9           outputting the results, said results identifying ones of said voltages not in  
10 compliance with IR and EM limits of said design.

11           14. A program storage device readable by a machine, tangibly embodying a  
12 program of instructions executable by the machine to perform method steps of  
13 performing power distribution analysis for I/O circuits in an integrated circuit (IC)  
14 design, said I/O circuits having defined placement locations within a power distribution  
15 network of said design, comprising the steps of:

1           a) calculating maximum and average currents for each of said I/O circuits,  
2 and an average logic current demand per node;

3           b) creating a resistance model of said power distribution network comprising  
4 nodes and resistors corresponding to points on buses of said network and resistivities  
5 corresponding to said points;

6           c) indexing each of said I/O circuit currents and said average logic current  
7 demand per node to the node in said model closest to the corresponding I/O circuit  
8 location;

9           d) solving the resistance and current source model resulting from step (c) for  
10 voltages at the nodes; and

16 e) outputting the results.

1 15. A computer system comprising:  
2 a memory containing computer-executable instructions;  
3 a processor coupled to said memory for executing said instructions, said  
4 instructions when executed performing a process comprising:  
5 from a power distribution network for an IC design, generating a resistance model  
6 comprising resistivities at nodes corresponding to said network;  
7 relating currents of I/O circuits connected to said network, and an average logic  
8 current demand per node, to nodes in said resistance model;  
9 solving for voltages at said nodes in terms of said resistivities, I/O circuit currents  
10 and average logic current demand per node; and  
11 outputting the results, said results identifying ones of said voltages not in  
12 compliance with IR and EM limits of said design.